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(54) A semiconductor device and a method of manufacturing it

Specification

(57)(Abstract)

(Subject)

To provide a method of manufacturing a semiconductor device, and a semiconductor device manufactured by the process wherein the reduction of memory cell capacitor surface caused by miniaturization is minimized, without the use of a masking process.

(Means to Solve the Problem)

Conducting film is self-alignigly patterned to form capacitor electrodes by forming a conducting pillar that protrudes upward from an interlayer insulating film, depositing a conducting film on the conducting pillar, and by performing anisotropic etching, utilizing the unevenness of the conducting film that that appears as a consequence of the existence of the conducting pillar.

(Claims)

(Claim 1)

A method of manufacturing a semiconductor device provided with a capacitor, wherein the method of manufacturing the semiconductor device, comprises the processes of

(A) forming an insulating film on a substrate;

(B) forming a conducting pillar so that it protrudes upward from the insulating film;

(C) depositing a first conducting film on the insulating film, so that it covers the conducting pillar;

(D) forming a capacitor electrode by applying anisotropic etching to the first conducting film, the etching acting substantially perpendicularly to the principle surface of the substrate;
(E) depositing a dielectric film on the capacitor electrode; and
(F) depositing a second conducting film on the dielectric film, to form a capacitor.
(Claim 2)
The method of claim 1, wherein the conducting pillar penetrates the insulating film, and electrically contacts a diffused region that is formed on the top of the substrate.
(Claim 3)
The method of claim 1 or 2 wherein, in the process in (D), the anisotropic etching is continued until the capacitor electrode is spatially separated from an adjacent capacitor electrode.
(Claim 4)
The method of any one of claims 1 – 3, wherein between the processes (A) and (B) additionally a process is provided for covering the surface of the insulating film with an etching stopper layer which becomes a stopper with respect to the etching that acts on the insulating film, the anisotropic etching in process (D) being carried out until the etching stopper layer is exposed.
(Claim 5)
The method of any one of claims 1 – 4, wherein additionally, a process is included for forming hemispherical polysilicon grains on the electrode pattern, and the process in (E) is executed so that the dielectric film covers the hemispherical polygon grains.
(Claim 6)
A method of manufacturing a semiconductor provided with a capacitor, wherein the method of manufacturing the semiconductor device, comprises the processes of
forming an interlayer insulating film on a substrate;
forming a first conducting film on the interlayer insulating film;
penetrating the conducting film and the interlayer insulating film and forming a conducting pillar, so that the pillar protrudes upward from the surface of the first conducting film;
depositing a first insulating film on the conducting pillar following the shape of the conducting pillar;
forming a first insulating sleeve from a first insulating film by applying a first anisotropic etching to the first insulating film, the etching acting substantially perpendicularly to the principle surface of the substrate until the top surface of the pillar and the first conducting film are exposed;
after the first anisotropic etching process, depositing a second conducting film on the first conducting film, so as to cover the first insulating sleeve and the top surface of the pillar;
forming a first conducting sleeve on the outside of the first insulating sleeve by applying a second anisotropic etching to the second conducting film, the etching acting substantially perpendicularly to the principle surface of the substrate until the surface of the interlayer insulating film is exposed;
selectively etching the first insulating sleeve so as to remove it, leaving the pillar and the first conducting sleeve so that the first conducting sleeve surrounds the pillar, separated from it by a space;
depositing a dielectric film on the surface of the pillar and the surface of the first conducting sleeve; and
depositing a third conducting film, which constitutes a counter electrode film, on the dielectric film.
(Claim 7)
The method of claim 6 wherein the pillar is formed of a hollow sleeve, and the process of depositing the dielectric film is carried out so that the dielectric film covers the surface of the inner wall of the hollow sleeve.
(Claim 8)
The method of claim 6 or 7 wherein, after the second anisotropic etching process, and prior to the selective etching process, are included the processes of
depositing a fourth conducting film and a second insulating film sequentially on the surface of the interlayer insulating film, so as to include the first pillar, and the first conducting sleeve and the first insulating sleeve, which surround the pillar;
forming a second insulating sleeve from the second insulating film by means of applying a third anisotropic etching to the second insulating film, the etching acting substantially perpendicularly to the principle surface of the substrate, until the fourth conducting film is exposed;
depositing a fifth conducting film on the fourth conducting film so as to include the second insulating sleeve, fourth conducting film, and the pillar;

applying anisotropic etching sequentially to the fifth and fourth conducting films, the etching acting substantially perpendicularly to the principle surface of the substrate until the surface of the interlayer insulating film is exposed, forming from the fourth conductive film, a second conducting sleeve that is attached to the first conducting sleeve, forming from the second insulating film, a second insulating sleeve that surrounds the second conducting sleeve, and forming from the fifth conducting film, a third conducting sleeve that surrounds the second insulating sleeve,
the processes being included, so that in the selective etching process the second insulating sleeve and the first insulating sleeve are removed substantially simultaneously.
(Claim 9)
A semiconductor device comprising a substrate in which is formed a diffused region, an interlayer insulating film formed on the substrate, a contact hole formed in the interlayer insulating film and exposing the diffused region, and a capacitor that contacts the diffused region via the contact hole, wherein the semiconductor device is one wherein the capacitor comprises
a conducting pillar extending through the contact hole, one end contacting the diffused region, and the other end protruding from the interlayer film forming a protruding portion;
a storage electrode that electrically contacts the protruding portion of the conducting pillar;
a capacitor dielectric film formed on the storage electrode; and
a counter electrode formed on the capacitor dielectric film.
(Claim 10)
The semiconductor device of claim 9 wherein an etching stopper layer that is capable of substantially preventing the etching of the material that forms the interlayer insulating film, is formed on the surface of the interlayer insulating film.
(Claim 11)
The semiconductor device of claim 9 or 10, wherein the surface of the storage electrode has an irregular form.
(Claim 12)
The semiconductor device of any on one of claims 9 – 11, wherein the conducting pillar comprises of a hollow sleeve formed with an interior wall surface, and the capacitor dielectric film covers the surface of the interior wall of the conducting pillar.
(Claim 13)
The semiconductor device of claim 9, wherein the storage electrode closely contacts the protruding portion of the pillar.
(Claim 14)
The semiconductor device of claim 9 wherein the storage electrode comprises the conducting pillar itself, and one or a plurality of conducting sleeves that surround the conducting pillar, and the capacitor dielectric film covers the protruding portion of the conducting pillar and the surfaces the conducting sleeve or the plurality of conducting sleeves.
(Claim 15)
The semiconductor device of claim 14 wherein the conducting pillar and the conducting sleeve or plurality of sleeves are mutually electrically connected via a conducting film that is formed on the surface of the interlayer insulating film.
(Claim 16)
A semiconductor device comprising
a semiconductor substrate;
a word line electrode formed separated from the surface of the semiconductor substrate, by a gate oxide film that corresponds to a channel region;
a first diffused region formed in the semiconductor substrate, corresponding to one end of the channel region;
a second diffused region formed in the semiconductor substrate, corresponding to the other end of the channel region;
an interlayer insulating film formed on the semiconductor substrate, that covers the gate electrode, and the first and second diffused regions;
a first contact hole formed in the interlayer insulating film, that exposes the first diffused region;
a second contact hole formed in the interlayer insulating film, that exposes the second diffused region;
a memory cell capacitor that contacts the first diffused region via the first contact hole; and
a bit line electrode that contacts the second diffused region via the second contact hole;

wherein the semiconductor device is one wherein the memory cell capacitor comprises
a conducting pillar that extends through the first contact hole, one end contacting the first diffused region and the other end forming a protruding portion that protrudes above the interlayer insulating film;
a storage electrode formed on the interlayer insulating film, closely contacting the protruding portion of the pillar;
a capacitor dielectric film formed so as to cover the storage electrode; and
a counter electrode formed on the capacitor dielectric film.

Specification

(Detailed Description of the Invention)
(0001)
(Field of the Invention)
The invention relates to general semiconductor devices. In particular it relates to a semiconductor device that includes a capacitor, and a method of manufacturing the semiconductor device that includes a capacitor. Due to miniaturization, the memory capacity of semiconductor devices, and in particular semiconductor memory devices such as DRAM that include capacitors, is increasing every year. In particular, in the case of DRAM, information is stored as an electrical charge in memory cell capacitors. However as the result of miniaturization memory cell capacitors have become minute, which reduces the electrical charge that is stored in the capacitors, making it difficult to determine whether the memorized information is 1 or 0.
(0002)
Therefore, studies have been made concerning a DRAM construction and a method of DRAM manufacture wherein, although the device pattern of the semiconductor device is miniaturized, capacitance is reduced as little as possible.
(0003)
(Related Art)
Fig 13 (A) – (C) and Fig 14 (D), (E) describe typical, conventional DRAM manufacturing processes. Referring to Fig 13 (A), an oxide film 2 that includes a field oxide film 2A is formed on the active area of p type Si substrate 1, the field oxide film 2A forming an image of an active region. N+ type diffused regions 1A. 1B, and 1C are formed in the active region as in the case of a normal memory cells. Additionally a polysilicon gate pattern 3 extends above the oxide layer 2.
(0004)
The gate pattern 3 is covered by an oxide film 3A, and an interlayer insulating film 4 of BPSG covers above that. A contact hole 4A, which exposes the diffused region 1B, is formed in the interlayer insulating film 4. A polysilicon bit line pattern 5 contacts the diffused region 1B via the contact hole 4A. Additionally, in the condition shown in Fig 13 (A), another BPSG interlayer insulating film 6 is formed on the interlayer insulating film 4, so as to bury the bit line pattern 5.
(0005)
Next, in the process shown in Fig 13 (B). contact holes 6A are formed that penetrate both the interlayer insulating films 4 and 6, exposing the diffused regions 1A or 1C. Also, in the process in Fig 13 (C) a polysilicon or amorphous silicon layer 7 is deposited on the interlayer insulating film 6 so as to fill the contact holes 6A. In the process in Fig 13 (C), additionally. a resist pattern 8 is formed on the layer 7. In the process in Fig 14 (D) the layer 7 is patterned using the resist pattern 8 as a mask. In this way a capacitor electrode pattern 7A is formed on the interlayer insulating film 6.
(0006)
Next, in the process in Fig 14 (E) a dielectric film 9 is formed on the capacitor electrode pattern 7A, and a polysilicon film 10 is deposited on that.
(0007)
(Problems to be solved by the invention)
Fig 15 is a top view that shows an array of the capacitor electrode pattern 7A on the interlayer insulating film 6. Referring to Fig 15, the electrode pattern 7A is not a regular rectangle, but has rounded corners. This is due to the fact that when miniaturizing to increase DRAM integration density while at the same time attempting to assure sufficient memory cell capacitor capacitance, the space between the electrodes 7A inevitably becomes extremely small. Therefore, when forming the resist pattern 8 in the processes in Fig 13 C, exposure must be performed near the resolution

limit of high-resolution lithography. That is, conventionally, in the case of exposure, resolution limitations place restrictions on the intervals between the electrodes 7A, which in the case of miniaturizing DRAM, causes a problem with the dimensions of the electrodes 7A, and therefore with securing sufficient surface area.

(0008)

Additionally, using the conventional method shown in Figs 13(A) – 14(E), a large number of processes are required due to the use of the resist pattern 8. This causes problems in that it increases the cost of manufacture and at the same time reduces semiconductor device manufacture throughput. The overall object of the invention is to provide a semiconductor device and its manufacturing process wherein the abovementioned problems are solved.

(0009)

In particular, the object of the invention is to provide a structure for a semiconductor device and a method of its manufacture wherein. even if the device is miniaturized, sufficient capacitance will be ensured for the memory cell capacitors. A further object of the invention is to provide a manufacturing method wherein, in the case of manufacturing a semiconductor device so that even if the device is miniaturized sufficient capacitance will be ensured for the memory cell capacitors, memory cell capacitors can be formed without a masking process.

(0010)

(Means to Solve the Problem)

The invention solves the problems by means of the following.

As stated in claim 1, by a method of manufacturing a semiconductor device provided with a capacitor, wherein the method of manufacturing the semiconductor device, comprises the processes of

(A) forming an insulating film on a substrate;

(B) forming a conducting pillar so that it protrudes upwardly from the insulating film;

(C) depositing a first conducting film on the insulating film, so that it covers the conducting pillar;

(D) forming a capacitor electrode by applying anisotropic etching to the first conducting film, the etching acting substantially perpendicularly to the principle surface of the substrate;

(E) depositing a dielectric film on the capacitor electrode; and

(F) depositing a second conducting film on the dielectric film, to form a capacitor.

Or, as stated in claim 2, by the method of claim 1, wherein the conducting pillar penetrates the insulating film. and electrically contacts a diffused region that is formed on the top of the substrate.

Or, as stated in claim 3, by the method of claim 1 or 2 wherein, in the process in (D), the anisotropic etching is continued until the capacitor electrode is spatially separated from an adjacent capacitor electrode.

Or, as stated in claim 4, by the method of any one of claims 1 – 3, wherein between the processes (A) and (B) additionally a process is provided for covering the surface of the insulating film with an etching stopper layer which becomes a stopper with respect to the etching that acts on the insulating film. the anisotropic etching in process (D) being carried out until the etching stopper layer is exposed.

Or, as stated in claim 5, by the method of any one of claims 1 – 4, wherein additionally, a process is included for forming hemispherical polysilicon grains on the electrode pattern, and the process in (E) is executed so that the dielectric film covers the hemispherical polygon grains.

Or, as stated in claim 6. by a method of manufacturing a semiconductor provided with a capacitor, wherein the method of manufacturing the semiconductor device, comprises the processes of

forming an interlayer insulating film on a substrate;

forming a first conducting film on the interlayer insulating film;

penetrating the conducting film and the interlayer insulating film and forming a conducting pillar, so that the pillar protrudes upward from the surface of the first conducting film;

depositing a first insulating film on the conducting pillar following the shape of the conducting pillar;

forming a first insulating sleeve from a first insulating film by applying a first anisotropic etching to the first insulating film, the etching acting substantially perpendicularly to the principle surface of the substrate until the top surface of the pillar and the first conducting film are exposed;

after the first anisotropic etching process. depositing a second conducting film on the first conducting film, so as to cover the first insulating sleeve and the top surface of the pillar;

forming a first conducting sleeve on the outside of the first insulating sleeve by applying a second anisotropic etching to the second conducting film, the etching acting substantially perpendicularly to the principle surface of the substrate until the surface of the interlayer insulating film is exposed;
selectively etching the first insulating sleeve so as to remove it, leaving the pillar and the first conducting sleeve so that the first conducting sleeve surrounds the pillar, separated from it by a space;
depositing a dielectric film on the surface of the pillar and the surface of the first conducting sleeve; and
depositing a third conducting film, which constitutes a counter electrode film, on the dielectric film.
Or, as stated in claim 7, by the method of claim 6 wherein the pillar is formed of a hollow sleeve, and the process of depositing the dielectric film is carried out so that the dielectric film covers the surface of the inner wall of the hollow sleeve.
Or, as stated in claim 8, by the method of claim 6 or 7 wherein, after the second anisotropic etching process, and prior to the selective etching process, are included the processes of
depositing a fourth conducting film and a second insulating film sequentially on the surface of the interlayer insulating film, so as to include the first pillar, and the first conducting sleeve and the first insulating sleeve, which surround the pillar;
forming a second insulating sleeve from the second insulating film by means of applying a third anisotropic etching to the second insulating film, the etching acting substantially perpendicularly to the principle surface of the substrate, until the fourth conducting film is exposed;
depositing a fifth conducting film on the fourth conducting film so as to include the second insulating sleeve, fourth conducting film, and the pillar;
applying anisotropic etching sequentially to the fifth and fourth conducting films, the etching acting substantially perpendicularly to the principle surface of the substrate until the surface of the interlayer insulating film is exposed, forming from the fourth conductive film, a second conducting sleeve that is attached to the first conducting sleeve, forming from the second insulating film, a second insulating sleeve that surrounds the second conducting sleeve, and forming from the fifth conducting film, a third conducting sleeve that surrounds the second insulating sleeve,
the processes being included, so that in the selective etching process the second insulating sleeve and the first insulating sleeve are removed substantially simultaneously.
Or, as stated in claim 9, by a semiconductor device comprising a substrate in which is formed a diffused region, an interlayer insulating film formed on the substrate, a contact hole formed in the interlayer insulating film and exposing the diffused region, and a capacitor that contacts the diffused region via the contact hole, wherein the semiconductor device is one wherein the capacitor comprises
a conducting pillar extending through the contact hole, one end contacting the diffused region, and the other end protruding from the interlayer film forming a protruding portion;
a storage electrode that electrically contacts the protruding portion of the conducting pillar;
a capacitor dielectric film formed on the storage electrode: and
a counter electrode formed on the capacitor dielectric film.
Or, as stated in claim 10, by the semiconductor device of claim 9 wherein an etching stopper layer that is capable of substantially preventing the etching of the material that forms the interlayer film, is formed on the surface of the interlayer insulating film.
Or, as stated in claim 11, by the semiconductor device of claim 9 or 10, wherein the surface of the storage electrode has an irregular form.
Or, as stated in claim 12, by the semiconductor device of any on one of claims 9 – 11, wherein the conducting pillar comprises of a hollow sleeve formed with an interior wall surface, and the capacitor dielectric film covers the surface of the interior wall of the conducting pillar.
Or, as stated in claim 13, by the semiconductor device of claim 9, wherein the storage electrode closely contacts the protruding portion of the pillar.
Or, as stated in claim 14, by the semiconductor device of claim 9 wherein the storage electrode comprises the conducting pillar itself, and one or a plurality of conducting sleeves that surround the conducting pillar, and the capacitor dielectric film covers the protruding portion of the conducting pillar and the surfaces the conducting sleeve or the plurality of conducting sleeves.
Or, as stated in claim 15, by the semiconductor device of claim 14 wherein the conducting pillar and the conducting sleeve or plurality of sleeves are mutually electrically connected via a conducting film that is formed on the surface of the interlayer insulating film.

Or. as stated in claim 16, by a semiconductor device comprising
a semiconductor substrate;
a word line electrode formed separated from the surface of the semiconductor substrate, by a gate oxide film that corresponds to a channel region;
a first diffused region formed in the semiconductor substrate, corresponding to one end of the channel region;
a second diffused region formed in the semiconductor substrate, corresponding to the other end of the channel region;
an interlayer insulating film formed on the semiconductor substrate, that covers the gate electrode, and the first and second diffused regions;
a first contact hole formed in the interlayer insulating film, that exposes the first diffused region;
a second contact hole formed in the interlayer insulating film, that exposes the second diffused region;
a memory cell capacitor that contacts the first diffused region via the first contact hole; and
a bit line electrode that contacts the second diffused region via the second contact hole;
wherein the semiconductor device is one wherein the memory cell capacitor comprises
a conducting pillar that extends through the first contact hole, one end contacting the first diffused region and the other end forming a protruding portion that protrudes above the interlayer insulating film;
a storage electrode formed on the interlayer insulating film. closely contacting the protruding portion of the pillar;
a capacitor dielectric film formed so as to cover the storage electrode; and
a counter electrode formed on the capacitor dielectric film.

(0011)

The principle of the invention is described referring to Figs 1 (A) – (C). In the invention, first, in the process in Fig 1 (A), an interlayer insulating film 12 is deposited on a semiconductor substrate 11 in which are formed diffused regions 11A, 11B. Additionally the surface of the interlayer insulating film 12 is covered with an etching stopper layer 12C. Next, an insulating film (not shown) is deposited on this, and contact holes 12A and 12B are formed, penetrating the insulating film (not shown) and the interlayer insulating film 12, to expose respectively the diffused regions 11A and 11B. Furthermore, after the contact holes 12A and 12B are filled with a conductor such as polysilicon, the insulating film above the etching stopper layer 12C is removed, forming conducting pillars 12A, 12B that protrude upward from the interlayer insulating film 12. Additionally a conducting film 13 of polysilicon or amorphous silicon is deposited so as to cover the conducting pillars 12A, 12B.

(0012)

Next, in the process in Fig 1(B). anisotropic etching, operating substantially perpendicularly to the principle surface of the substrate 11, is performed on the conducting film 13. until the etching stopper layer 12C is exposed, dividing the conducting film 13 into electrode patterns 13A and 13B. Additionally, in the process in Fig 1(C), a dielectric film 14 and a conducting film 15 are sequentially deposited, on the structure of Fig 1(B). making it possible to form mutually adjacent capacitors C1 and C2, without any masking process other than the masking process used to form the contact holes 12A, 12B. Because the patterns 13A and 13B are formed in this way without a masking process, the problems of alignment error or exposure resolution limitations that are associated with the masking process do not occur, making it possible to reduce the interval D between the patterns 13A, 13B substantially more than the interval D in Fig 13(C).

(0013)

(Embodiments of the Invention)

Embodiment 1

Figs 2(A) – (D) and 3(E) – (G) show a DRAM memory cell manufacturing process according to embodiment 1 of the invention. Referring to Fig 2(A), an oxide film 22 that includes a field oxide film 22A is formed on the active region on a p type Si substrate 21, the field oxide film 22A forming an image of the active region. n+ type diffused regions 21A, 21B, 21C are formed in the active region in the same way that normal memory cells are formed, and additionally a gate pattern 23 of polysilicon extends on the oxide film 22, the gate pattern 23 constituting a word line pattern to the memory cells in the usual manner.

(0014)

The gate pattern 23 is covered with an oxide film 23A, which in turn is covered by an interlayer insulating film 24 of BPSG. A contact hole 24A, which exposes the diffused region 21B, is formed in the interlayer insulating film 24 by means of dry etching wherein an mixture of CHF3, CF4, and Ar is used in a parallel plane etcher at an RF frequency of 380kHz. Then a polysilicon bit line pattern 25 contacts the diffused region 21B via the contact hole 24A. Furthermore, in the condition in Fig (A), another BPSG interlayer insulating film 26 is formed on the interlayer insulating film 24, so as to bury the bit line pattern 25. Also, an etching stopper layer 27, which acts as an etching stopper for the interlayer insulating film 26, and another insulating film 28, are deposited sequentially on the film 26. Typically the interlayer insulating film 24 and the insulating film 28 are formed of a film of BPSG, or SiO2 that is deposited by high-density plasma CVD. On the other hand, the etching stopper layer 27 is formed of an SiN film, typically formed to a thickness of 22nm.

(0015)

Next, in the processes in Fig 2(B), contact holes 26A and 26B respectively are formed by means of high-resolution photolithography that employs a resist, penetrating the films 24 – 28 so as to expose the diffused regions 21A and 21C. Additionally in the processes in Fig 2(C) the contact holes 26A and 26B are filled with conducting polysilicon, and the polysilicon film that remains above the insulating layer 28 is selectively removed. Thus conducting plugs 27A and 27B are obtained that fill the contact holes 26A and 26B.

(0016)

Also, in the processes in Fig 2(D) the structure of Fig 2(C) is wet etched in a solution of HF or buffered HF, removing the insulating film 28 selectively with respect to the etching stopper layer 27, and as a result the conducting plugs 27A, 27B protrude upward from the etching stopper layer 27. Next, in the processes in Fig 3(E), a conducting amorphous or polysilicon film 29 is uniformly deposited on the structure of Fig 2(D). Additionally anisotropic etching is performed on the polysilicon film 29 obtained in Fig 3(E), acting in a direction substantially parallel to the principle surface of the substrate 21, using for example an ECR etching device in a gaseous mixture of Cl2 and O2. In this case, anisotropic etching is performed until the etching stopper layer 27 is exposed, and as a result, as shown in Fig 3(F), the capacitor electrode patterns 29A and 29B are formed from the conducting film 29.

(0017)

In the anisotropic etching process of Fig 3(F) vertical anisotropism governs. However, it is also possible to perform quasi-anisotropic etching that also etches in the horizontal direction. This is also the same for embodiments that are described below. Also, in the embodiment, a thermally oxidized film is formed on the capacitor electrode patterns 29A and 29B of Fig 3(F), and an SiN film 30 is deposited thereon. Then, after the surface of the SiN film 30 is thermally oxidized, a polysilicon film 31 is uniformly deposited so as to cover the electrode patterns 29A, 29B as a counter electrode. In the construction, the dielectric film 30, in conjunction with the thermally oxidized film below and above, forms a so-called ONO structure, and the electrode patterns 29A. 29B both form the storage electrodes of DRAM memory cell capacitors.

(0018)

The storage electrode patterns 29A, 29B that are formed by the method, are formed using neither photolithography, nor a masking process. Therefore, the interval between the patterns can be reduced with no limitation from the resolution of an exposure system. Also, with the embodiment the only exposure that requires high resolution is the photolithography process for forming the contact holes 26A, 26B. Also the exposure used for the storage electrode patterns 29A, 29B does not use a masking process. Therefore semiconductor device manufacturing throughput is greatly improved.

(0019)

In the abovementioned description the conducting pillars 13A, 13B, or the deposited conducting film 13, is given as being comprised of amorphous silicon or polysilicon that from the beginning has been doped with conducting impurities. However, the invention is not limited to the particular embodiment, and it is also possible to deposit undoped amorphous silicon or polysilicon and subsequently introduce impurities to provide conductivity. This is also true for the other embodiments that are described below.

Embodiment 2

Fig 4 shows the construction of a DRAM memory cell according to embodiment two of the invention. The same reference symbols have been attached for previously described sections and their description is omitted.

(0020)

Referring to Fig 4, in the embodiment a rough surface structure 290 is formed on the surface of the storage electrode patterns 29A, 29B using substantially hemispherical polysilicon grains (HSG: hemispherical grained polysilicon), and the capacitor dielectric film 30 is formed so as to cover the roughened surface structure 290. Forming the roughened surface 290, increases the surface areas of the storage electrode patterns 29A, 29B, and as a result the capacitance of the memory cell capacitors increases.

(0021)

The hemispherical polysilicon grains do not generally have a geometrically perfect hemispherical shape; they are deformed, having irregular forms such as a mushroom shape with a constricted base, etc. However, in the invention these irregular polysilicon grains will also be called hemispherical polysilicon grains. To form such a roughened surface structure 290, for example the storage electrode pattern is formed in an amorphous silicon state, and then on it is formed a polysilicon film of, for example, the raw ingredient SiH4, depositing at a temperature of substantially 570°C. Depositing a polysilicon film on an amorphous silicon film causes heterogeneous nucleation on the surface of the amorphous silicon. As a result, hemispherical polysilicon grains grow heterogeneously on the storage electrode patterns 29A, 29B. The formation of such rough surfaces is described in for example. "Growth Mechanism of Polycrystalline Si Films with Hemispherical Grains", Oto Buturi[1] Vol. 61, No. 11, 1992, Tatsumi Et Al.

Embodiment 3

Next a method of manufacturing DRAM memory cells according to embodiment 3 of the invention will be described referring to Figs 5(A) – (C) and Figs 6(D) – (F). However, of the items in Figs 5(A) – (C) and Figs 6(D) – (F) sections that correspond to those mentioned above have the same symbols attached, and their descriptions are omitted. Furthermore, in this embodiment, of the previously described construction, only the section that includes the diffused region 21C and the conducting plug 27B will be described.

(0022)

Referring to Fig 5(A). the interlayer insulating film 26 of the embodiment also includes the previously described insulating film 24, and a polysilicon conducting film 27A is formed between the etching stopper layer 27 and the insulating film 28. It follows that in the embodiment the contact hole 26B extends. penetrating through the layers 26, 27, 27A. and 28, and the conducting plug 27B fills the contact hole 26B that penetrates the layers 26, 27, 27A, and 28.

(0023)

Next, in the processes in 5(B), in the same manner as in the process in Fig 2(D) above, the insulating film 28 is removed by etching selectively with respect to the conducting film 27A. Additionally. an SiO2 film 32 is CVD deposited on the conducting layer 27A so as to cover the conducting plug 27B that protrudes from the film 27A. Next, in the processes in Fig 5(C), a dry etching process is applied to the SiO2 film 32, acting substantially perpendicularly to the substrate 21. By performing the dry etching process until the conducting film 27A is exposed, the SiO2 film 32 only remains on the side wall surface of the pillar 27B in the form of a sleeve 32A.

(0024)

Also, in the process in Fig 6(D). a conducting film 33 of polysilicon or amorphous silicon is CVD deposited on the construction of Fig 5[2](C). In the process in Fig 6(E) anisotropic etching is performed on the conducting film 33, acting substantially perpendicularly to the principle surface of the substrate 21, until the etching stopper layer 27 is exposed. the conducting film 33 remaining in the form of a conducting sleeve 33A. only on the outer surface of the insulating sleeve 32A.

(0025)

Next, in the processes in Fig 6(F), the construction of Fig 6(E) is immersed in an HF solution, dissolving and removing the insulating sleeve 32A. As the result of removing the insulating sleeve

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[1] The web site spells it like this. It means Applied Physics. Here is a synopsis of the article http://www.jsap.or.jp/ap/1992/ob6111/p611147.html#e

[2] Maybe mistake for 6?

32A, a space is formed between the conducting pillar 27B and the conducting sleeve 33A. However, in the embodiment, a capacitor dielectric film 30 is formed on the exposed surfaces of the conducting pillar 27B and the conducting sleeve 30[3]. The conducting pillar 27B and the conducting sleeve 33A are electrically connected by the conducting film that constituted part of the conducting film 27A.

(0026)

Also, in the processes in Fig 6(F) a polysilicon or amorphous silicon conducting film is deposited as a counter electrode 31 on the capacitor dielectric film 30 so as to fill the space. A memory cell capacitor of the same construction is also formed for the diffused region 21A. In the embodiment, it is possible to increase the surface area of the memory cell capacitor, and therefore the capacitance, without using a masking process.

Embodiment 4

Fig 7 shows part of a DRAM memory cell according to embodiment 4 of the invention. As in the previous embodiment, it only shows the construction of the memory cell capacitor that is connected to the diffused region 21C. Also, sections that correspond to previously described sections have the same symbols attached, and their descriptions are omitted.

(0027)

Referring to Fig 7, in the embodiment, another conducting sleeve 36A is formed, outside of the conducting sleeve 33A and spaced separated from the sleeve 33A. The capacitor dielectric film 30 is formed not only on the exposed surfaces of the conducting pillar 27B and the conducting sleeve 33A, but also on the exposed surfaces of the conducting sleeve 36A. However, the conducting sleeve 36A is electrically connected to the conducting sleeve 33A and the conducting pillar 27B by the polysilicon or amorphous silicon conducting film that is on the etching stopper layer 27. Also, the counter electrode 31 is deposited so as to also fill in the space between the conducting sleeves 33A and 36A.

(0028)

In the embodiment it is possible to increase the number of conducting sleeves that compose the memory cell capacitor, and as a result it is possible to increase the surface area of the capacitor dielectric film, and therefore the capacitance. Next, referring to Figs 8(A), (B) and 9(C), (D), the method of manufacturing the capacitor structure in Fig 7 will be described. However, sections in the diagrams that have been previously described have the same symbols attached, and their descriptions are omitted.

(0029)

Referring to Fig 8(A), a polysilicon or amorphous silicon conducting film 34 and an SiO2 insulating film 35 are deposited in order on the structure in Fig 6(E). Next, in the process in Fig 8(B) anisotropic etching is performed on the insulating film 35, acting substantially in a direction perpendicular to the principle surface of the substrate 21, until the conducting film 34 is exposed. As a result of the anisotropic etching, an insulating sleeve 35A is formed from the insulating film 35 so as to surround the conducting film 34 from the outside.

(0030)

Also, in the processes in Fig 9(C) another polysilicon or amorphous silicon conducting film 36 is deposited on the structure of Fig 8(B). In the process in Fig 9(D) anisotropic etching is performed, acting substantially perpendicularly to the principle surface of the substrate 21, on the conducting layer 36 and the conducting film 34 that is below it, until the etching stopper layer 27 is exposed, thus forming the structure in Fig 9(D). In the structure in Fig 9(D) as a result of the anisotropic etching, the conducting film 34 is held, sandwiched between the insulating sleeve 35A and the conducting sleeve 33A, forming a conducting sleeve 34A, and the conducting film 36 forms a conducting sleeve 36A, which is the section that is most external.

(0031)

The structure in Fig 9(D) is again immersed in an HF solution, etching to selectively remove the insulating sleeves 32A, 35A. A dielectric film 30 is deposited on the resultant structure, and additionally a counter electrode 31 is deposited, thus obtaining a capacitor having the structure shown in Fig 7.

Embodiment 5

[3] Mistake for 33A?

Fig 10 shows part of a DRAM memory cell according to embodiment 5 of the invention. As in the previous embodiment, it only shows the memory cell capacitor that is connected to the diffused region 21C. Also, sections that correspond to previously described sections have the same symbols attached, and their descriptions are omitted.

(0032)

Referring to Fig 10, a memory cell capacitor according to the embodiment has the same structure as the structure of the memory cell capacitor shown in Fig 7, except that the conducting pillar 27B is a hollow sleeve. Because of this, the capacitor dielectric film 30 is formed so as to cover not only the external wall surfaces of the conducting pillar, but also its inner wall surface and bottom surface. With the construction, because the surface area of the capacitor dielectric film 30 increases, the preferable characteristic of increased capacitance is obtained.

(0033)

Figs 11(A) – (C) and 12 (D) – (F) show the method of forming the structure shown in Fig 10. However, sections in the diagrams that have been previously described have the same symbols attached, and their descriptions are omitted. As Fig 11(A) shows, in the embodiment, in the contact hole 26B that penetrates the layers 26 – 28, instead of the conducting pillar of the process in Fig 5(A), a conducting sleeve 27B is deposited on the surface of the inner wall of the contact hole 26[4] and on the bottom portion of the contact hole 26[5] so as to cover the surface of the exposed diffused region 21C. Furthermore, in the process in Fig 11(B), after the insulating film 28 is removed by selective etching in HF, an SiO2 film 32 is deposited so as to fill the space inside the conducting sleeve 27B.

(0034)

Also, in the process in Fig 11(C) anisotropic etching is performed on the SiO2, acting in a direction substantially perpendicular to the principle surface of the substrate 21, until the conducting film 27A is exposed. This obtains the structure shown in Fig 11(C) in which the inside of the conducting sleeve 27B is filled with an SiO2 plug 32C and its outside is covered with an SiO2 insulating sleeve 32A.

(0035)

Next, in the process in Fig 12(D), a polysilicon or amorphous silicon conducting film 33 is deposited on the structure shown in Fig 11(C). Additionally, in the process in Fig 12(E) anisotropic etching is performed on the conducting film 33, acting in a direction substantially perpendicular to the principle surface of the substrate 21, until the etching stopper 27 is exposed, thus obtaining the structure shown in resin[6] 12(E), in which a conducting sleeve 33A is formed on the outside of the insulating sleeve 32A.

(0036)

The structure shown in Fig 12(E) is immersed in an HF solution, dissolving and removing the SiO2 plug 32C and the insulating sleeve 32A. Additionally a capacitor dielectric film 30 is deposited, and furthermore a counter electrode 31 is deposited on it, thus obtaining the structure shown in Fig 12(F). At the stage of Fig 12(E), by performing the processes shown in Figs 8(A), (B), Figs 9(C), (D), it is possible to arbitrarily increased the number of conducting sleeves that surround the conducting sleeve 27B and that together with the conducting sleeve 27B form a storage electrode.

(0037)

In embodiment 3 and subsequent embodiments, the conducting film 27A becomes an etching stopper for the insulating film 28. Therefore the SiN etching stopper layer 27 is not necessarily required, and may be omitted. Also, although in the invention, the interlayer insulating films 24, 26 are BPSG, it is also possible to use other SiO2 or polyimide deposited in a planar, insulating-film high-density plasma.

(0038)

Although the above, is a description of a preferred embodiment, the invention is not limited by the embodiments. Various changes in shape, and modifications may be made within the essence that is described in the claims.

(0039)

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[4] Seem to have omitted the B
[5] Seem to have omitted the B
[6] Must be a typo for Fig.

(Benefits of the invention)
In the invention of claims 1 – 4 and 9, 10, and 13 a method of manufacturing a semiconductor device comprising with a capacitor, is performed, comprising the processes of
(A) forming an insulating film on a substrate;
(B) forming a conducting pillar so that it protrudes upwardly from the insulating film;
(C) depositing a first conducting film on the insulating film, so that it covers the conducting pillar;
(D) forming a capacitor electrode by applying anisotropic etching to the first conducting film, the etching acting substantially perpendicularly to the principle surface of the substrate;
(E) depositing a dielectric film on the capacitor electrode; and
(F) depositing a second conducting film on the dielectric film, to form a capacitor.
Therefore, it is possible to self alignigly form a large number of capacitors without using a masking process, and without the resolution limitations that accompany the masking process, and therefore at a minimum interval. Accordingly it is possible to suppress to a minimum the reduction in capacitor surface area, and therefore capacitance, that is caused by miniaturization. Also, because the invention does not use a masking process, it is possible to greatly improve throughput in the manufacture of semiconductors.

(0040)
In the invention of claims 5 and 11, additionally, a process is performed for forming hemispherical polysilicon grains on the electrode pattern, and the process in (E) is executed so that the dielectric film covers the hemispherical polygon grains.
Therefore it is possible to increase the surface area and the capacitance of the formed capacitor.

(0041)
In the invention of claim 6, 14, and 15, a method of manufacturing a semiconductor provided with a capacitor, is performed, comprising the processes of
forming an interlayer insulating film on a substrate;
forming a first conducting film on the interlayer insulating film;
penetrating the conducting film and the interlayer insulating film and forming a conducting pillar, so that the pillar protrudes upward from the surface of the first conducting film;
depositing a first insulating film on the conducting pillar following the shape of the conducting pillar;
forming a first insulating sleeve from a first insulating film by applying a first anisotropic etching to the first insulating film, the etching acting substantially perpendicularly to the principle surface of the substrate until the top surface of the pillar and the first conducting film are exposed;
after the first anisotropic etching process, depositing a second conducting film on the first conducting film, so as to cover the first insulating sleeve and the top surface of the pillar;
forming a first conducting sleeve on the outside of the first insulating sleeve by applying a second anisotropic etching to the second conducting film, the etching acting substantially perpendicularly to the principle surface of the substrate until the surface of the interlayer insulating film is exposed;
selectively etching the first insulating sleeve so as to remove it, leaving the pillar and the first conducting sleeve so that the first conducting sleeve surrounds the pillar, separated from it by a space;
depositing a dielectric film on the surface of the pillar and the surface of the first conducting sleeve; and
depositing a third conducting film, which constitutes a counter electrode film, on the dielectric film.
Therefore, it is possible, without using a masking process, to self-alignigly construct the storage electrode from the conducting pillar and a large number of conducting sleeves that surround the conducting pillar, greatly increasing the surface area of the capacitor dielectric film, and therefore the capacitance of the capacitor.

(0042)
In the invention of claims 7 and 12, the pillar is made to be a hollow sleeve.
Therefore it is possible to further increase the capacitance of the capacitor.
In the invention of claim 8,
after the second anisotropic etching process, and prior to the selective etching process,
a fourth conducting film and a second insulating film are sequentially deposited on the surface of the interlayer insulating film, so as to include the first pillar, and the first conducting sleeve and the first insulating sleeve, which surround the pillar;

a second insulating sleeve is formed from the second insulating film by means of applying a third anisotropic etching to the second insulating film, the etching acting substantially perpendicularly to the principle surface of the substrate, until the fourth conducting film is exposed;
a fifth conducting film is deposited on the fourth conducting film so as to include the second insulating sleeve, fourth conducting film, and the pillar;
an anisotropic etching process is sequentially applied to the fifth and fourth conducting films, the etching acting substantially perpendicularly to the principle surface of the substrate until the surface of the interlayer insulating film is exposed, forming from the fourth conductive film, a second conducting sleeve that is attached to the first conducting sleeve, forming from the second insulating film, a second insulating sleeve that surrounds the second conducting sleeve, and forming from the fifth conducting film, a third conducting sleeve that surrounds the second insulating sleeve, and additionally in the selective etching process the second insulating sleeve is removed at substantially the same time as the first insulating sleeve.
Therefore it is possible to freely increase the number of conducting sleeves that surround the conducting pillar, self-aligningly, and without using a masking process.
(0043)
In the invention according to claim 16 a semiconductor device is constructed of
a semiconductor substrate;
a word line electrode formed separated from the surface of the semiconductor substrate, by a gate oxide film that corresponds to a channel region;
a first diffused region formed in the semiconductor substrate, corresponding to one end of the channel region;
a second diffused region formed in the semiconductor substrate, corresponding to the other end of the channel region;
an interlayer insulating film formed on the semiconductor substrate, that covers the gate electrode, and the first and second diffused regions;
a first contact hole formed in the interlayer insulating film, that exposes the first diffused region;
a second contact hole formed in the interlayer insulating film, that exposes the second diffused region;
a memory cell capacitor that contacts the first diffused region via the first contact hole; and
a bit line electrode that contacts the second diffused region via the second contact hole;
wherein the semiconductor device is one wherein the memory cell capacitor comprises
a conducting pillar that extends through the first contact hole, one end contacting the first diffused region and the other end forming a protruding portion that protrudes above the interlayer insulating film;
a storage electrode formed on the interlayer insulating film, closely contacting the protruding portion of the pillar;
a capacitor dielectric film formed so as to cover the storage electrode; and
a counter electrode formed on the capacitor dielectric film.
Therefore, it is possible to self-aligningly form DRAM memory cells in which there is little reduction in the capacitance of the memory cell capacitors, even when miniaturized, without using a masking process.

Description of the Drawings

(Simple Description of the Drawings)
Fig 1 (A) – (C): Diagrams that describe the principle of the invention.
Fig2 (A) – (D): Part one of diagrams that describe the manufacturing process for a semiconductor device according to embodiment 1 of the invention.
Fig 3 (E) – (G): Part two of diagrams that describe the manufacturing process for a semiconductor device according to embodiment 1 of the invention.
Fig 4: A diagram that describes the construction of a semiconductor device according to embodiment 2 of the invention.
Fig 5 (A) – (C): Part one of diagrams that describe the manufacturing process for a semiconductor device according to embodiment 3 of the invention.
Fig 6 (D) – (F): Part two of diagrams that describe the manufacturing process for a semiconductor device according to embodiment 3 of the invention.

Fig 7: A diagram that describes the construction of a semiconductor device according to embodiment 4 of the invention.
Fig 8 (A), (B): Part one of diagrams that describe the manufacturing process for a semiconductor device according to embodiment 4 of the invention.
Fig 9 (C), (D): Part two of diagrams that describe the manufacturing process for a semiconductor device according to embodiment 4 of the invention.
Fig 10: A diagram that describes the construction of a semiconductor device according to embodiment 5 of the invention.
Fig 11 (A) – (C): Part one of diagrams that describe the manufacturing process for a semiconductor device according to embodiment 5 of the invention.
Fig 12 (D) – (F): Part two of diagrams that describe the manufacturing process for a semiconductor device according to embodiment 5 of the invention.
Fig 13 (A) – (C): Part one of diagrams that describe the conventional manufacturing process for a semiconductor device.
Fig 14 (D), (E): Part two of diagrams that describe the conventional manufacturing process for a semiconductor device.
Fig 15: Diagram that shows a top view of the shape of a memory cell capacitor that is formed by the conventional method.

(Description of the Symbols)

1, 11, 21: Substrates
1A, 1B, 1C, 11A, 11B, 21A, 21B, 21C: Diffused regions
2, 22: Gate oxide films
2A, 22A: Field oxide films
3, 23: Gate electrodes (word lines)
3A, 23A: Insulating films
4, 6, 24, 26: Interlayer insulating films
5, 25: Bit lines
6A, 12A, 12B, 26A, 26B: Contact holes
7, 13, 29 Conducting layers
7A, 13A, 13B, 29A, 29B: Storage electrode patterns
8, 14, 30: Dielectric films
10, 15, 31: Counter electrodes
12A, 12B, 27A, 27B: Conducting pillars
12C, 27: Etching stoppers
28: Insulating film
290: Rough surface construction
32, 35: Insulating films
32A, 35A: Insulating sleeves
32C: Insulating plug
33, 34, 36: Conducting films
33A, 34A, 36A: Conducting sleeves